ABSTRACT OF DISCLOSURE

A thin film transistor array panel is provided, which includes: a substrate; a gate electrode; a gate insulating layer formed on the gate electrode; a polysilicon layer formed on the gate insulating layer and including a pair of ohmic contact areas doped with conductive impurity; source and drain electrodes formed on the ohmic contact areas at least in part; a passivation layer formed on the source and the drain electrodes and having a contact hole exposing the drain electrode at least in part; and a pixel electrode formed on the passivation layer and connected to the drain electrode through the contact hole.